Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Layer 1 - Top Layer	Copper	1.40mil		
4	Dielectric 1	370HR	5.20mil	4.2	
5	Layer 2 - GND	Copper	1.42mil		
6	Dielectric 2	370HR	43.00mil	4.2	
7	Layer 3 - PWR	Copper	1.42mil		
8	Dielectric 3	370HR	5.20mil	4.2	
9	Layer 4 - Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

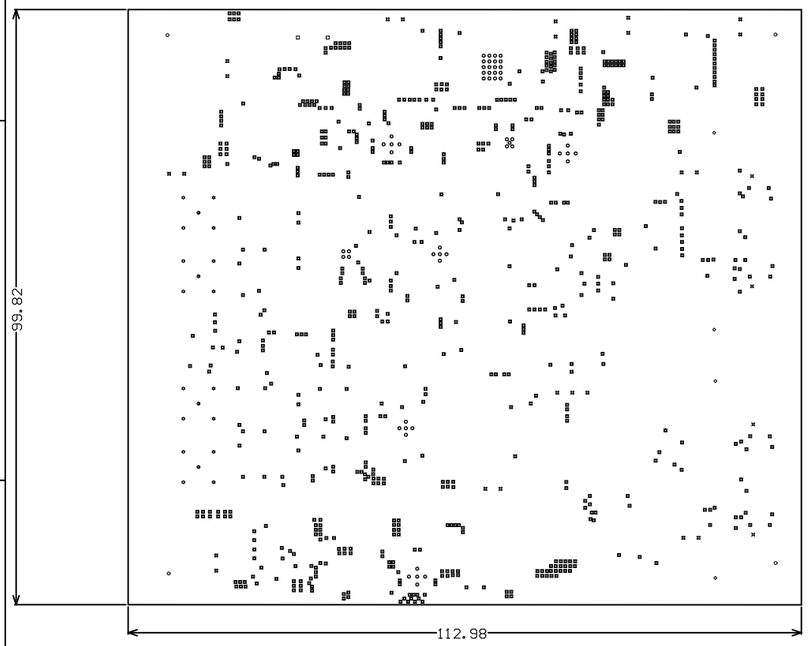
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: .127 mm
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

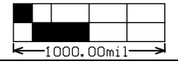
MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER





Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
✖	4	40.00mil (1.016mm)	NPTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
◇	4	173.23mil (4.400mm)	NPTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
✪	54	7.87mil (0.200mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
◙	730	10.00mil (0.254mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
⊠	23	45.28mil (1.150mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
□	2	51.18mil (1.300mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
●	4	59.06mil (1.500mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
✡	16	66.93mil (1.700mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Layer 1 - Top Layer - Layer 4 - Bottom Layer	
	841 Total					

TEXAS INSTRUMENTS

PROJECT TITLE: ADC Voltage Reference Buffer Optimization Reference Design for
DESIGNED FOR: Public Release
FILE NAME: TIDA-01055.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01055	REV: E1	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: 01055		
PLOT NAME = Fabrication Drawing	GENERATED : 8/4/2017 12:30:31 PM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Taras Dudar & Dylan Hubbard	
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.1.12.290